IN THE SPECIFICATION

The paragraph beginning on page 11, line 10 has been amended to read as follows:

B1

--FIG.'s **3A** and **3C** are block circuit diagrams illustrating a first testing method for testing the connection between an IP (chip IP) and wiring according to the first embodiment.--

The paragraph beginning on page 11, line 13 has been amended to read as follows:

B2

--FIG.'s **3B** and **3D** are block circuit diagrams illustrating a second testing method for testing the connection between an IP (chip IP) and wiring according to the first embodiment.--

The paragraph beginning on page 15, line 1 has been amended to read as follows:

B3

--A feature of the present embodiment is the provision of test pads **27**, **28**, **33** and **34** connected respectively to the wires **25**, **26**, **31** and **32**, which are connected to the circuit of the IP **24** whose electrical connection is to be tested. The wires **25**, **26**, **31** and **32** are provided in the form of the wiring layers **13** and **14** as illustrated in FIG. **1C**, and the test pads **27**, **28**, **33** and **34** are connected respectively to the wires **25**, **26**, **31** and **32** via contacts. The wire **25** is connected to a node **43a** of the circuit connected to an internal circuit **43** in the IP **24**, and the wire **26** to a ground line **41** in the IP **24**. The wire **31** is connected to a power supply line **42** in the IP **24**, and the wire **32** to a node **43b** of the internal circuit **43** in the IP **24**.--

The paragraph beginning on page 16, line 23 and ending on page 17, line 9, has been amended as follows:

--As illustrated in FIG. **3C**, when testing the electrical connection between the wires **25** and **26** and the IP **24**, a positive voltage is applied from a test pin **36** via the test pad **28** to the ground line **41** in the IP **24**. If the electrical connection is good, a forward current flows, by a forward voltage, from a protection diode to a node **43a** of the internal circuit **43** of the IP **24**. Therefore, by detecting a current or by detecting a voltage according to a voltage drop using a test pin **35**, it is possible to determine the condition of the electrical connection between the IP and the wire in the silicon wiring substrate (for example, the condition of the connection between pads shown by broken lines in the figure) based on the measured voltage or current value.--

B4

The paragraph beginning on page 17, line 12 and ending on page 18, line 9, has been amended as follows:

--FIG. **3B** is a block circuit diagram illustrating a second testing method for testing the connection between an IP (chip IP) and wiring. As illustrated in the figure, a selector **44** is provided in the IP **24**. The selector **44** receives, and selectively outputs one of, the output of the internal circuit **43** of the IP **24** and a power supply voltage VDD (ground voltage VSS), which is the output of the power supply line **42** (the ground line **41**). When testing the electrical connection between the wires **31** and **32** and the IP **24**, a logic voltage (e.g., H) such that the output of the power supply line **42** is selected is supplied to the selector **44** from the wire **32** via the test pad **34**. Then, if the electrical connection is good, the power supply voltage VDD is output to the test pin **37** via the test pad **33**. Therefore, the condition of the electrical connection can be determined by

B5